

What is claimed is:

1. A semiconductor apparatus comprising:
a signal providing circuit which provides
an input signal set including at least one input
signal;
5 a data analyzer outputting a digital result
signal in synchronization with a clock signal;
wherein said data analyzer inverts said digital
result signal at a timing indicated by said clock
signal while said input signal set is in a
10 predetermined state, and does not invert said
digital result signal while said input signal set
is not in said predetermined state.
2. The semiconductor apparatus according to
claim 1, wherein said input signal set includes
first and second digital signals, and said
predetermined state is a coincident state in
5 which said first and second digital signal
coincide with each other.
3. The semiconductor apparatus according to
claim 1, wherein said data analyzer includes:
a logic circuit outputting a flip-flop
input signal in response to said input signal set,
5 and
a flip-flop latching said flip-flop input

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signal to store a storage datum, and outputting said digital result signal in response to said storage datum, and

10 said logic circuit outputs said flip-flop input signal so as to appear an inverse of said storage datum while said input signal set is in a predetermined state, and outputs said flip-flop input signal so as to indicate said storage datum
15 while said input signal set is not in a predetermined state.

4. The semiconductor apparatus according to claim 3, wherein said at least one input signal is digital, and said logic circuit comprises:

an inverter which receives said storage
5 datum and outputs an inverted signal indicative of an inverse of said storage datum, and

an exclusive OR gate outputting said flip-flop input signal so as to indicate an exclusive OR of said at least one input signal and said
10 inverted signal.

5. A semiconductor apparatus comprising:

a set of n comparators which is responsive to $2n$ input signals for outputting n digital result signals, wherein an i -th comparator (i
5 being an natural number not more than n) of said

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n comparator is responsive to a $(2i-1)$ -th input signal and a $2i$ -th input signal of said $2n$ input signals for outputting an i -th digital result signal of said n digital result signals in
10 synchronization with a clock signal; and

an OR gate outputting a total result signal indicative of an OR of said n digital result signals, wherein

said i -th comparator inverts said i -th
15 digital result signal at a timing indicated by said clock signal while said $(2i-1)$ -th input signal and said $2i$ -th input signal coincide with each other, and does not invert said digital result signal while said $(2i-1)$ -th input signal
20 and said $2i$ -th input signal do not coincide with each other.

6. A semiconductor apparatus comprising:

a set of n comparators which is responsive to $2n$ input signals for outputting n digital result signals, wherein an i -th comparator (i
5 being an natural number not more than n) of said n comparator is responsive to a $(2i-1)$ -th input signal and a $2i$ -th input signal of said $2n$ input signals for outputting an i -th digital result signal of said n digital result signals in
10 synchronization with a clock signal; and

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an AND gate outputting a total result signal indicative of an AND of said n digital result signals, wherein

15 said i-th comparator inverts said i-th digital result signal at a timing indicated by said clock signal while said (2i-1)-th input signal and said 2i-th input signal coincide with each other, and does not invert said digital result signal while said (2i-1)-th input signal
20 and said 2i-th input signal do not coincide with each other.

7. A semiconductor apparatus comprising:
an address generator which provides a tested memory with an address;

a test pattern generator which provides
5 said test memory with a test pattern to have an access to said address, and generates an expected pattern expected to be outputted from said tested memory;

a comparator which compares an output
10 pattern from said tested memory with said expected pattern to output a digital result signal in synchronization with a clock signal;
wherein said comparator inverts said digital result signal at a timing indicated by said clock
15 signal while said output pattern coincides with

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said expected pattern, and does not invert said digital result signal while said output pattern does not coincide with said expected pattern.

8. The semiconductor apparatus according to claim 7, wherein said tested memory and said semiconductor apparatus are embedded in a single semiconductor chip.

9. A semiconductor apparatus comprising:
a plurality of test circuits, each of which includes:

an address generator which provides a
5 tested memory with an address,

a test pattern generator which provides
said test memory with a test pattern to have an
access to said address, and generates an expected
pattern expected to be outputted from said tested
10 memory, and

a comparator which compares an output
pattern from said tested memory with said
expected pattern to output a digital result
signal in synchronization with a clock signal,
15 said comparator inverting said digital result
signal at a timing indicated by said clock signal
while said output pattern coincides with said
expected pattern, and not inverting said digital

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result signal while said output pattern does not
20 coincide with said expected pattern; and

an OR gate outputting a total result signal
indicative of an OR of said digital result signal.

10. The semiconductor apparatus according to
claim 9, wherein said tested memory and said
semiconductor apparatus are embedded in a single
semiconductor chip.

11. A semiconductor apparatus comprising:
a plurality of test circuits, each of which
includes:

an address generator which provides a
5 tested memory with an address,

a test pattern generator which provides
said test memory with a test pattern to have an
access to said address, and generates an expected
pattern expected to be outputted from said tested
10 memory, and

a comparator which compares an output
pattern from said tested memory with said
expected pattern to output a digital result
signal in synchronization with a clock signal,
15 said comparator inverting said digital result
signal at a timing indicated by said clock signal
while said output pattern coincides with said

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expected pattern, and not inverting said digital
result signal while said output pattern does not
20 coincide with said expected pattern; and

an AND gate outputting a total result
signal indicative of an AND of said digital
result signal.

12. The semiconductor apparatus according to
claim 11, wherein said tested memory and said
semiconductor apparatus are embedded in a single
semiconductor chip.

13. A method of operating a semiconductor
apparatus, comprising:

providing an input signal set including at
least one input signal;

5 outputting a digital result signal in
response to said input signal set in
synchronization with a clock signal; wherein said
digital result signal is inverted at a timing
indicated by said clock signal while said input
10 signal set is in a predetermined state, and is
not inverted while said input signal set is not
in said predetermined state.

14. A method of testing a circuit, comprising:

inputting an output pattern from said

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inputting an expected pattern to said
semiconductor apparatus, said expected pattern
being expected to be outputted from said circuit;

outputting a digital result signal by said

10 semiconductor apparatus in response to said
output pattern and said expected pattern in
synchronization with said clock signal, wherein
said digital result signal is inverted at a
timing indicated by said clock signal while said
15 output pattern coincides with said expected
pattern, and is not inverted while said output
pattern does not coincide with said expected
pattern.